WHAT IS CLAIMED IS:

1. A driver circuit, comprising:

a differential first pair of transistors;

a voltage drive stage comprising a second pair of transistors;

a first pair of nodes coupled to the first pair of transistors and to the second pair of transistors;

a second pair of nodes coupled to the second pair of transistors; and

a dynamic current switch coupled to the second pair of nodes.

2. The driver circuit of claim 1 further comprising a first pair of resistors coupled to the first pair of nodes.

3. The driver circuit of claim 2 further comprising a voltage regulator coupled to the first pair of resistors.

4. The driver circuit of claim 1 further comprising a load resistor coupled to the second pair of nodes.

5. The driver circuit of claim 1 further comprising a second pair of resistors coupled to the second pair of nodes.

6. The driver circuit of claim 5 further comprising a pair of output nodes coupled to the second pair of resistors.

7. The driver circuit of claim 5 further comprising an output voltage coupled to the second pair of resistors.

8. The driver circuit of claim 1 further comprising three serially coupled transistor and resistor pairs, wherein the first serially coupled transistor is coupled to an input node, wherein the second serially coupled transistor is coupled to the

differential first pair of transistors, and wherein the third serially coupled transistor comprises a portion of the dynamic current switch.

9. The driver circuit of claim 8, wherein the first transistor is coupled to the second transistor.

10. The driver circuit of claim 8, wherein the second transistor is coupled to the third transistor.

11. The driver circuit of claim 8, further comprising a ground, wherein the three resistors of the serially coupled transistor and resistor pairs, are coupled to the ground.

12. The driver circuit of claim 8, further comprising a transistor coupled to the input node.

13. The driver circuit of claim 1, wherein a first one of the first pair of nodes follows a first one of the second pair of nodes.

14. The driver circuit of claim 1, wherein a second one of the first pair of nodes follows a second one of the second pair of nodes.

15. The driver circuit of claim 1, further comprising a pair of input nodes coupled to the differential first pair of transistors and to the dynamic current switch.

16. A circuit, comprising:

a voltage drive stage comprising a pair of transistors;

a dynamic current switch coupled to the voltage drive stage; and

a load resistor coupled to the pair of transistors;

wherein current conducted through the pair of transistors are closely matched.

17. A method of limiting current in a driver circuit having a pair of input nodes coupled to a differential first pair of transistors, a voltage drive stage comprising a second pair of transistors, a first pair of nodes coupled to the first pair of transistors and to the second pair of transistors, a second pair of nodes coupled to the second pair of transistors, and a dynamic current switch coupled to the second pair of nodes, the method comprising:

conducting a current through one of the second pair of transistors when one of the input nodes, one of the first pair of nodes, and one of the second pair of nodes is high; and

conducting the current through the dynamic current switch.

18. The method of claim 17, wherein the current conducted through the dynamic current switch is greater than a current conducted through a load resistor coupled to the second pair of nodes.

19. The method of claim 18 further comprising conducting current through another one of the second pair of nodes.

20. The method of claim 19 further comprising contemporaneously conducting the current through the one of the second pair of nodes and the current through the other one of the second pair of nodes.

21. The method of claim 19, wherein the current conducted through the other one of the second pair of nodes is equal to the current conducted through the dynamic current switch minus the current conducted through the load resistor.

22. The method of claim 19, wherein the current conducted through the other one of the second pair of nodes is smaller than the current conducted through the load resistor.

23. The method of claim 19, wherein the current conducted through the one of the second pair of nodes and the current conducted through the other one of the second pair of nodes are closely matched.

24. The method of claim 17, wherein the second pair of transistors are closely matched.

25. A method of limiting current in a circuit having a voltage drive stage comprising a pair of transistors and a dynamic current switch comprising a pair of tri-state switches coupled to a serially coupled transistor and resistor pair and to the pair of transistors, the method comprising:

contemporaneously conducting current through the pair of transistors;

conducting current through at least one of the pair of tri-state switches; and

conducting current through the dynamic current switch.

26. The method of claim 25, wherein the current conducted through the dynamic current switch is equal to the current conducted through the at least one of the pair of tri-state switches.